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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/700,033	11/03/2003	Greory William Smaus	5500-91600	3398

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EXAMINER	
JOHNSON, BRIAN P	

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
11/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/700,033	SMAUS ET AL.	
	Examiner	Art Unit	
	Brian P. Johnson	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-23 are pending.

Papers Filed

2. Examiner acknowledges receipt of amendments and remarks filed on 07 December 2006.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 8-12, 15, and 18-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Peled (U.S. Patent No. 6,216,206).

1. Regarding claims 1, 8, 15, and 23 Peled discloses a microprocessor, comprising: a system memory (col 1 lines 21-23), an instruction cache (col 3 lines 8-9 and fig. 1 reference 105); a trace cache (col 3 lines 26-27 and fig 2 reference 230); and a prefetch unit coupled to the instruction cache and the trace cache;

Note that an instruction is required to be instructions within the cache memory must be fetched from the cache to be executed; therefore, a fetch to this cache memory is considered to be a "prefetch". The component of the processor that completes this functionality is considered to be a "prefetch unit".

wherein the prefetch unit is configured to fetch instruction code from a system memory for storage within the instruction cache (col 1 lines 21-23), and wherein the prefetch unit is further configured to fetch a line of instructions into the instruction cache in response to a trace being evicted from the trace cache (col 7 lines 50-52).

2. Regarding claims 7, 14 and 18, Peled discloses the microprocessor of claims 1 and 8, wherein the prefetch unit is configured to inhibit the fetch of a line of instructions into the instruction cache in response to the eviction of certain traces from trace cache if the evicted trace is predicted unlikely to re-execute (col 7 lines 42-46).

3. Regarding claims 2, 3, 9, 10, 19 and 20, Peled discloses the processor of claims 1, 8 and 15, wherein the prefetch unit is configured to fetch a line into the instruction cache comprising instructions that correspond to operations that precede and follow a branch in the evicted trace (col 1 lines 12-42).

4. Regarding claims 4, 11 and 21, Peled discloses the microprocessor of claims 1, 8 and 15, wherein the prefetch unit is configured to prefetch a plurality of lines of instructions into the instruction cache in response to the trace being evicted from the trace cache (col 2 lines 15-17 and col 1 lines 21-23).

5. Regarding claims 5, 12, and 22, Peled discloses the microprocessor of claims 4, 11, and 21, wherein the prefetch unit is configured to fetch a number of lines that is

proportional to the number of branch operations comprised in the evicted trace (col 1 lines 12-42).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 6, 7, 13, 14,16 and 17 rejected under 35 U.S.C. 103(a) as being unpatentable over Peled in view of prior art.

8. Regarding claims 6 and 13, Peled discloses the microprocessor of claims 1 and 8.

Peled fails to disclose a cache that checks for duplicate information within the cache to inhibit the storing said duplicate information.

Examiner takes Official Notice that it would have been obvious at the time of the invention for one of ordinary skill in the art to take the invention of Peled and utilize a cache system that, when presented with information to store, checks if that information already exists and inhibits duplicate storage. IN particular, within the invention of Peled, the combination would check when there is an eviction from the trace cache.

Regarding the motivation, Examiner asserts that this technique is extremely common practice within cache systems. Storing the same information within different

portions of a cache is a waste of resources that can create a detriment to the processing system with regards to space, cost, power and speed.

9. Regarding claims 7 and 14, Peled discloses the microprocessor of claims 1 and 8, wherein the prefetch unit is configured to inhibit the fetch of a line of instructions into the instruction cache in response to the eviction of certain traces from the trace cache if the evicted trace is predicted unlikely to re-execute.

Note that, as explained in the reference, a victim cache takes items removed from the main cache. The algorithm may later place that item back in the main cache and, later yet, remove it again. In this circumstance the cache would check the victim cache and inhibit the fetching of this item, because it is already there.

10. Regarding claim 16, Peled discloses the method of claim 15, further comprising checking the instruction cache for lines of instructions comprising the instructions corresponding to the evicted trace.

Nothing that the instruction cache accepts victim traces upon removal (col 7 lines 50-52) and that the cache checks for duplicate entries (as combined), the limitation above appropriately follows.

11. Regarding claim 17, Peled discloses the method of claim 16, further comprising inhibiting the fetching of the line of instructions into the instruction cache if the line of instructions is stored in the instruction cache.

The functionality of claim 17 follows the combination as described above.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4174. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RICHARD L. ELLIS
PRIMARY EXAMINER